## REMARKS

Claims 1-12 are pending in the present application. Claims 1, 2 and 7 have been amended. Claims 13-20 have been canceled.

## Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority Under 35 U.S.C. 119 and receipt of the certified copy of the priority document.

## Drawings

Enclosed is one (1) drawing Annotated Sheet, wherein Fig. 15 has been corrected to indicate "Reg [7:0]", as described beginning on page 21, line 10 of the present application. Also enclosed is one (1) drawing Replacement Sheet incorporating the above noted correction. **The Examiner is respectfully requested to acknowledge receipt and acceptance of the drawing Replacement Sheet**.

## Claim Rejections-35 U.S.C. 112

Claims 13-20 have been rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the written description requirement. Although Applicant does not necessarily concede that this rejection is proper, claims 13-20 have been canceled merely to advance prosecution of this application. The Examiner is therefore respectfully requested to withdraw this rejection.

Claims 1-20 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. This rejection is respectfully traversed for the following reasons.

The arithmetic unit of claim 1 includes in combination a memory; an arithmetic logic unit "for executing a predetermined arithmetic operation with respect to a data from memory, the data being grouped into one of several patterns"; a register; and a combining circuit "for receiving a first output data from the arithmetic logic unit and a second output data from the register, and outputting data which is provided by replacing a part of the first output data and a part of the second output data based on the pattern of the data". As set forth, claim 1 makes clear first and second output data respectively provided from the arithmetic logic unit and the register.

Claim 7 has been amended in a somewhat similar manner, to include in combination among other features a combining circuit "for receiving a first output data from the arithmetic logic unit and a second output data from the register, and outputting data which is provided by replacing a part of the data read from memory with the first output data". As set forth, claim 7 makes clear first and second output data. Applicant respectfully submits that claims 1-12 are in compliance with 35 U.S.C. 112, second paragraph, and thus respectfully urges the Examiner to withdraw this rejection.

## Conclusion

The Examiner is respectfully requested to enter the above noted amendments which improve claim form and thus reduce the number of issues. The Examiner is

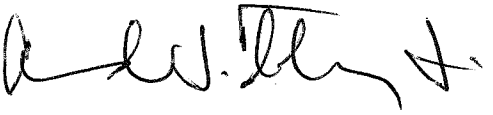
further respectfully requested to withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.



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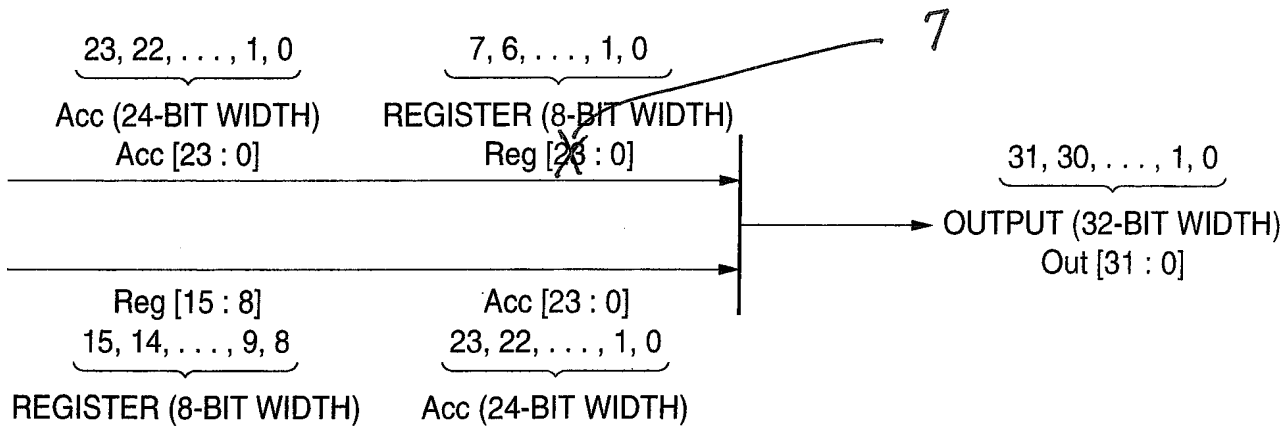
Enclosures: One (1) drawing Annotated Sheet
One (1) drawing Replacement Sheet

FIG. 15


7
23, 22, . . . , 1, 0
Acc (24-BIT WIDTH)
Acc [23 : 0]
7, 6, . . . , 1, 0
REGISTER (8-BIT WIDTH)
Reg [23 : 0]
31, 30, . . . , 1, 0
OUTPUT (32-BIT WIDTH)
Out [31 : 0]
Reg [15 : 8]
15, 14, . . . , 9, 8
REGISTER (8-BIT WIDTH)
Acc [23 : 0]
23, 22, . . . , 1, 0
Acc (24-BIT WIDTH)